UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/964,749	09/28/2001	Takumi Washio	WN-2387	3098

21254 7590 12/22/2004

MCGINN & GIBB, PLLC
8321 OLD COURTHOUSE ROAD
SUITE 200
VIENNA, VA 22182-3817

EXAMINER	
COLEMAN, ERIC	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 12/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/964,749	WASHIO, TAKUMI	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 9/30/04.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-19 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-19 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suetake (patent No. 5,742,842) in view of Roy (patent No. 6,065,092) or Sidman (patent No. 5,680,641).

2. Suetake taught the invention substantially as claimed including a data processing ("DP") system comprising:

a) Processor unit (CPU, 801) which controls processing of an operation (e.g., see fig.4, col. 11, lines 21-46);

b) Additional processing units each of which access to one of the memory banks and performs the operation independently of the processor unit, wherein the operation is performed about data stored in the particular memory bank based on an instruction or data provided from the processor unit (processing pipelines within the vector unit e.g., see fig. 10 and col. 11, line 55-col. 13, line 42).

3. Suetake did not expressly detail (claims 1,8,13,14-19) that the memory banks corresponded to the processor units or locking out access to the memory banks. First of all, Roy taught a memory with a plurality of independent clusters such that an access

arbitrated provides a locked out access to each of the corresponding memory banks (described as eight clusters)(e.g., see col. 22, lines 12-23) each of which comprised a separate memory bank and separate bus or data channel (e.g., see col. 9, line 31-col. 10, line 22) for independent access by separate processors (e.g., see col. 7, lines 17-49 and col. 10, lines 50-67) in parallel. Here this constituted a plurality of three or more memory banks that corresponded to the plurality of three or more processing units. Alternatively, Sidman taught register banks that corresponded to processing units with memory controller and locked out access to memory banks (e.g., see fig. 3) that comprised at least three corresponding banks and processing units e.g., see col. 10, lines 18-38).

4. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Roy and Suetake. One of ordinary skill would have been motivated to incorporate the Roy teachings of the independent access to memory banks at least to increase processing efficiency by reducing memory access latency.

5. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Sidman and Suetake. One of ordinary skill would have been motivated to incorporate the Sidman teachings of the parallel access to memory banks at least to increase processing efficiency by reducing memory access latency.

6. As per claim 2, Suetake taught the processing unit performing at least one of calculating the data, reading the data from the memory bank or writing the data to the memory bank (e.g., see col. 11, line 55-col. 13, line 42). Roy also taught processors capable of performing these operations (e.g., see col. 10, lines 50-67 of Roy). Sidman

also taught processors capable of performing these operations (e.g., see fig.3 of Sidman).

7. As per the additional limitations of claims 3,8,13,14 Suetake taught the address of the data in the memory bank was provided by the processor unit, and each of the additional processing units reads the data by referring to the address and performs the operation designated by the processor about the read data, and writes the result of the process into the location corresponding to the address (e.g., see col. 11, line 55-col. 13, line 42 and col. 17, lines 5-24).

8. As per claim 4,9, Suetake taught the additional processing unit received information from the processor unit and the operation designated by the processor was received information from the processor unit and operation designated by the processor was of the four basic operations of arithmetic, the additional processing unit performs one of the four basic operations using the read data and the received information (col. 11, line 55-col. 13, line 42).

9. As per claims 5, 10, the processing units of Sidman, Suetake and Roy each comprise processors that perform arithmetic operations in response to arithmetic instructions processing instructions. Arithmetic processing instructions, that add or subtract stored data to/from predetermined data (e.g., immediate operand), that read data from memory or registers and store the result in memory or registers indicated by and address within the instruction (e.g., indirect or direct arithmetic instructions) are well known in the DP art. Here Suetake Roy and Sidman taught processor for arithmetic processing one of ordinary skill would have been motivated to use conventional

arithmetic instructions to process data and store data in locations indicated within the instruction at least to simplify implementation for storage and retrieval of processing data.

10. As per claims 6,7,11,12, Suetake did not specify the particulars of the CPU in his system. However one of ordinary skill in the DP art would have been motivated to take advantage technological advances in the art at the time of the claimed invention namely selecting a CPU the processes instruction in parallel and which has the capability of processing vector data. This would have provided a system with more system processing capability for the vector data processed by the Suetake system.

Applicant's arguments with respect to claims 1-14 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Sidman (patent No. 6,029,242) disclosed a DP system using a shared register bank and a plurality of processors (e.g., see abstract).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EC

ERIC COLEMAN
PRIMARY EXAMINER